

SECURITY COPROCESSOR FOR ENHANCING COMPUTER SYSTEM SECURITY

Publication number: JP2001524229 (T)

Publication date: 2001-11-27

Inventor(s):

Applicant(s):

Classification:

- international: G06F12/14; G06F1/00; G06F9/38; G06F21/00; G06F21/22; G06F21/24; G06F12/14; G06F1/00; G06F9/38; G06F21/00; G06F21/22; (IPC1-7): G06F12/14; G06F1/00

- European: G06F21/00N3V8; G06F9/38S4; G06F21/00N1C1; G06F21/00N3P

Application number: JP19980535851T 19980210

Priority number(s): US19970799306 19970213; US19970799339 19970213; WO1998US02536 19980210

Also published as:

WO9836517 (A1)

EP1013023 (A1)

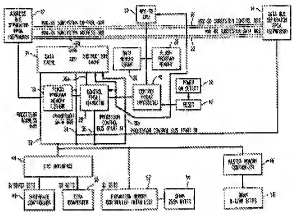
EP1013023 (B1)

AT308171 (T)

Abstract not available for JP 2001524229 (T)

Abstract of corresponding document: **WO 9836517 (A1)**

A security enhanced computer system arrangement includes a coprocessor (10) and a multiprocessor logic controller (38) inserted into the architecture of a conventional computer system. The coprocessor and multiprocessor logic controller is interposed between the CPU of the conventional computer system to intercept and replace control signals that are passed over certain of the critical control signal lines associated with the CPU. The CPU is released by allowing control signals to again pass between it and the computer system. Isolating the CPU control signal from the remainder of the computer system, allows a multiprocessor logic controller (38) to interrupt the normal computer system operation at any time and permit the coprocessor to check digital signatures of any firmware or software in the computer system. The multiprocessor logic controller arrangement thereby isolates the CPU of the conventional computer system from the remainder of the conventional computer system, permitting separate control over the CPU and separate control over the remainder of the computer system.



Data supplied from the **esp@cenet** database — Worldwide